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(54) Apparatus and methods for controlling firmware branch points in an electronic postage meter.

(57) For controlling firmware branch points in an electronic postage meter, a program is stored in ROM (14) for operation of the electronic postage meter, at least one data bit external to the stored program is stored in non-volatile memory (24), each such data bit corresponding to a particular branch point in the program, and a branch of the program is selected for use in operation of the meter in accordance with the data bit so that the program may be readily reconfigured based on the presence of a data bit.

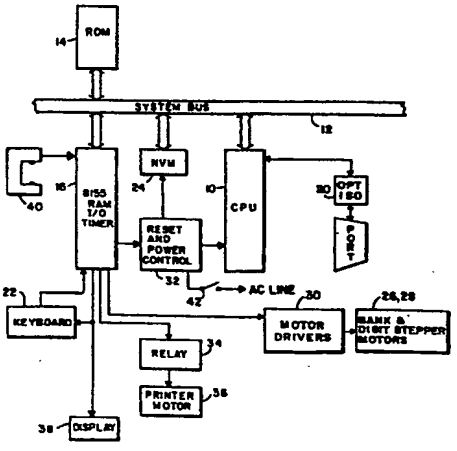


FIG. 1

EP 0 111 316 A2

Croydon Printing Company Ltd.

APPARATUS AND METHODS FOR CONTROLLING FIRMWARE BRANCH POINTS IN AN ELECTRONIC POSTAGE METER

The present invention relates to apparatus and methods for controlling firmware branch points in an electronic postage meter and to electronic postage meters.

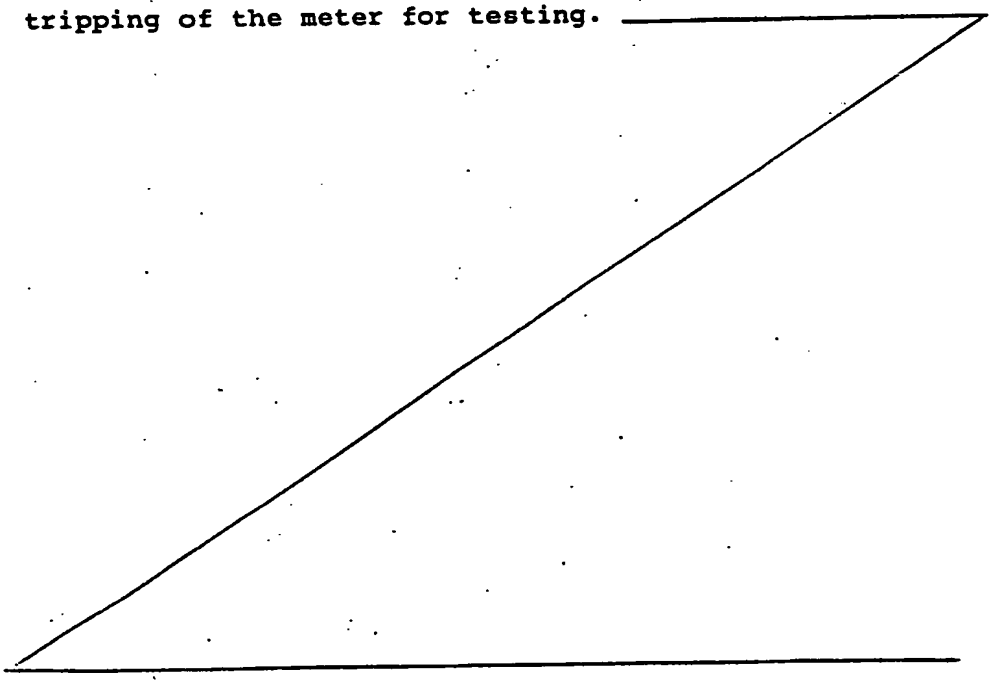
The present application is related to the copending European patent application of even date corresponding to U.S. Patent Application Serial No. 447,815, in the name of Danilo Buan, entitled "Stand-Alone Electronic Mailing Machine", which describes a postage meter within which the present invention may be utilized, and to the copending European patent application of even date corresponding to U.S. Patent Application Serial No. 447,912, in the names of John H. Soderberg and Edward C. Duwel, entitled "Modifying a Firmware Variable in an Electronic Postage Meter". The disclosures of both the above-mentioned applications are hereby incorporated herein by this reference.

A program listing for an electronic postage meter such as disclosed in the present application and in the aforementioned related patent application of Danilo Buan is set forth as part of this specification at the end of the detailed description and before the claims.

As stated above, the present invention relates broadly to electronic postage meters. An electronic postage

meter may operate under control of a program and include non-volatile memories (NVMs), such as the type disclosed in the aforementioned related patent applications.

Known electronic postage meters employing firmware such as disclosed in United States Letters Patent 4,301,507, issued on November 17, 1981, and assigned to Pitney Bowes, Inc. of Stamford, Connecticut are programmed via ROMs to undergo a certain sequence of operations. Such arrangement is adequate for use with a particular postal system such as that presently employed in the United States. However, for an electronic postage meter to be capable of international usage, where the requirements of the postal systems of the various countries vary widely, a number of individual programs or software packages tailored to the requirements of each country to accommodate such variations would increase the programming costs significantly. Further, even in the United States, it may be desirable to provide for external tripping of the meter for testing.



It is an object of the present invention to provide a program for an electronic postage meter which may be reconfigured for a particular application by information stored in the meter.

It is a further object of the present invention to provide a programmed electronic postage meter having a program which may be readily configured to satisfy a variety of postal systems.

It is a still further object of the present invention to provide an electronic postage meter having the same firmware for use in different postal systems.

It is another object of the present invention to provide a firmware controlled electronic postage meter for different applications in which programming costs are minimized.

Briefly, in accordance with the present invention, a method and apparatus for controlling firmware branch points in an electronic postage meter is provided comprising the steps of storing a program for operation of the electronic postage meter, providing at least one data bit external to the stored program, each such data bit corresponding to a particular branch point in the program, and selecting a branch of the program for use in operation of the meter in accordance with the data bit so that the program may be readily reconfigured based on the presence of a data bit.

Other objects, aspects and advantages of the present invention will be apparent from the detailed description considered in conjunction with the preferred embodiment of the invention illustrated in the drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a block diagram of the generalized electronic circuit for a stand-alone electronic postage meter;

FIGURE 2 formed from partial Figures 2a and 2b is a detailed block diagram of the electronic circuitry for a stand-alone electronic postage meter;

FIGURE 3 is a flowchart for reconfiguring the firmware to provide for a remote trip; and

FIGURE 4 is a flowchart for reconfiguring the firmware to reset the meter in accordance with its reset condition.

DETAILED DESCRIPTION

Referring to Figure 1, the electronic postage meter includes an 8-bit microprocessor 10 (CPU), such as an Intel Model 8085A microprocessor which is connected to various components through a system bus 12. ROM 14 is connected to the microprocessor 10 through the system bus 12. The ROM 14 stores the programs for controlling the postage meter. It should be understood that the term ROM as used herein includes permanently programmed and reprogrammable devices. An integrated circuit 16, which may be Intel Model 8155, is connected to the system bus 12 and includes RAM, input and output lines and a timer. The RAM portion of the intergrated circuit 16 has memory space allocated for transient storage of the data for the ascending register and descending register. An external data communication port 18 is connected to the microprocessor 10 through optical isolator 20. The external data communication port 18 allows connection with devices such as an electronic scale, an external computer, servicing equipment and the like. Also electrically connected to the microprocessor 10 through the system bus 12 is the keyboard 22 of the postage

meter and a non-volatile memory (NVM) 24. Stepper motors 26, 28 are also in electrical connection with the microprocessor 10 via motor drivers 30 and the integrated circuit 16. A reset and power control 32 is electrically connected between the integrated circuit 16, the NVM 24 and the microprocessor 10. A relay 34 connects the AC printer motor 36 to the integrated circuit 16. A display 38 is also electrically connected to the integrated circuit 16. Trip photosensor 40 is connected to the microprocessor 10 through integrated circuit 16 to indicate the presence of an envelope to be stamped, as described more fully in the aforementioned copending European patent application corresponding to the U.S. application entitled "Stand-Alone Electronic Mailing Machine".

The electronic postage meter is controlled by the microprocessor 10 operating under control of the programs stored in the ROM 14. The microprocessor 10 accepts information entered via the keyboard 22 or via the external communication port 18 from external message generators. Critical accounting data and other important information is stored in the non-volatile memory 24. The non-volatile memory 24 may be an MNOS semiconductor type memory, a battery augmented CMOS memory, core memory, or other suitable non-volatile memory component. The non-volatile memory 24 stores critical postage meter data during periods when power is not applied to the postage meter. This data includes in addition to the serial number of the mailing machine or postage meter information as to the value in the descending register (the amount of postage available for printing), the value in the ascending register (the total amount of postage printed by the meter), and the value in the piece count register (the total number of cycles the meter has performed), as well as other types of data, such as trip status, initialization and service information, which are desired to be retained in the memory even though no power is applied to the meter.

When an on/off power switch 42 is turned on (closed) a power supply internal to the mailing machine energizes

the microprocessor 10 and the balance of the electronic components. The information stored in the non-volatile memory 24 is transferred via the microprocessor 10 to the RAM of the integrated circuit 16. After power up the RAM contains an image or copy of the information stored in the non-volatile memory 24 prior to energization. During operation of the postage meter, certain of the data in the RAM is modified. Accordingly, when postage is printed, the descending register will be reduced by the value of the printed postage, the ascending register increased by the value of the printed postage and the piece counter register incremented. When the power switch 42 is turned off (opened), the updated data in the RAM is transferred via the microprocessor 10 back into a suitably prepared area of the non-volatile memory 24. A like transfer of information between the non-volatile memory 24 and the RAM takes place during power failure.

Referring to Figure 2, a more detailed block diagram of the arrangement of the electrical components for the postage meter is illustrated generally as 48. Power is supplied to the postage meter from the AC line voltage, typically 115 volts. This line voltage is applied to the meter through a hot switch 50 which cuts off power to the postage meter to protect the electrical components thereof if the temperature rises above a preset limit, nominally 70°C. The hot switch 50 is connected to the AC drive motor 36A through an RF filter 52 and an opto-triac 54 which provides isolation between the line voltage and the control logic for the meter. The hot switch 50 is also connected to a transformer 56 protected by a fuse 58. The output of the transformer 56 is coupled to a pre-regulator 59 through a cold switch 60. The cold switch 60 cuts off power to the pre-regulator 59 if the temperature drops below a preset limit, nominally 0°C. The pre-regulator 59 provides an output voltage of a predetermined range to a switcher 62 which generates the output voltage +5V; and the voltages for generating -12V and -30V.

The +5V is applied to a +3 volt regulator 64 and then to the

display 38A. The +5V from the switcher 62 is also applied to a +5V filter 66 which provides +5V for logic circuits. Specifically, the +5V is applied to the keyboard 22A, the display 38A, and bank, digit and trip sensor logic 68 and to the integrated circuits. The -12V is applied to a -12V regulator 70 and then to the non-volatile memory 24A.

The -30V output from the switcher 62 is also applied to a -30V regulator 74 and then to a -30V switch 76 which switches its output voltage on and off in response to the requirements of writing in NVM as dictated by the program. The output of the -30V switch is applied to the non-volatile memory 24A. The -30V supply is connected to the power on reset 72 of the microprocessor 10A.

+5V from the switcher 62 is also supplied to one input of the power on reset 72; the other input receives -30V from the regulator 74 as previously described. A low voltage sensor 88 also receives one input of +5V from the switcher 62 and its other input from the pre-regulator 59; its output is applied to the microprocessor 10A. The low voltage sensor 88 detects power failure and communicates this to the microprocessor 10A which in turn addresses the RAM through system bus 12A to transfer all security data present in the RAM to the non-volatile memory 24A.

Another output from the pre-regulator 59 in the form of +24V is applied to the digit and bank motor drive 30A for the bank motor 26A and digit motor 28A, which selects the particular printing wheel (bank) which is to be activated and the particular digit of the selected printing wheel which is to be set.

An output strobe from the integrated circuit 16A is buffered through buffer driver 68 and applied to digit sensor (encoder) 78, bank sensor (encoder) 80, and trip sensor 40A. The opto strobe

applies power to the digit sensor 78, bank sensor 80 and trip sensor 40A when needed. The output from the trip sensor 40A is applied to the input/output lines 82 which are coupled to the integrated circuit 16A. The outputs from the digit sensor 78 and bank sensor 80 and cycle switch 84 are applied to a storage buffer 86.

During power up, the key switch 42, see Figure 1, is closed, and the AC line voltage energizes the electrical components previously described and in Initialization process will occur. Such initialization may include a hard and/or soft initialization process as disclosed in the aforementioned United States Letters Patent 4,301,507. Preferably the Initialization process is that described in the copending European patent application of even date corresponding to U.S. Patent Application Serial No. 447,913, in the names of Alton B. Eckert and Easwaran C.N. Nambudiri entitled "Initializing the Print Wheels in an Electronic Postage Meter", and assigned to the present applicant. The disclosure of this copending European application is hereby incorporated herein by this reference.

In operation, the microprocessor 10A under control of the ROM 14A and possibly the auxiliary ROM 100 communicates over the address bus 94 and control bus 98 with the device select 98. The output of the device select 98 communicates with the particular module to be addressed over select lines 99. The modules to be addressed are the RAM, the ROM 14A, an auxiliary ROM 100, a demultiplexer 102, NVM logic 104 and the buffer 86. The RAM of integrated circuit 16A provides the working memory for the postage meter and the microprocessor 10A. The ROM 14A stores the program; the auxiliary ROM 100 may be used to provide additional program storage space.

The non-volatile memory 24A provides storage of all security information for the meter and retains such information during power down or power failure. The demultiplexer 102 latches the lower eight (8) bits of address information that defines a particular location which is used immediately thereafter. The NVM logic 104 controls the mode of operation of the NVM 24A and also provides ready wait and NVM ready signals to the microprocessor 10A to indicate the presence of the slow speed device (NVM) as active on the bus 12A.

Thus, the NVM logic 104 controls the data applied to the NVM 24A and also provides ready wait and NVM ready signals to the microprocessor 10A to advise it to wait for the NVM 24A or that the NVM 104 is ready to receive data over the data bus 108.

As previously mentioned, the digital sensor 78 (optical encoder) and bank sensor 80, (optical encoder) and cycle switch 84 whose current state is read, i.e., "Home" or "In Cycle", apply input signals to the storage latch 86 which sends output signals over data bus 108 to the microprocessor 10A for storage in the proper RAM location.

The RAM is also electrically coupled to I/O lines to transmit or receive data from the trip sensor 40A, the display 38A, keyboard 22A, and privilege access switch 110, if present. The privilege access switch 110 may be used in applications which require manual resetting of meter postage via a switch which is kept under seal.

A program listing for a postage meter of the type described in the aforementioned related patent application of Danilo Buan is set forth in the Program Appendix. The flow charts discussed below indicate how one or more external data bits preferably stored in non-volatile memory can be used to reconfigure those portions of the active software (firmware) stored in one or more ROMs. The program listing includes the code for the flow chart in Fig. 3, but only a portion of the code for the flow chart in Fig. 4.

Referring to Fig. 3, the flow chart for effecting an external trip via an external communication channel, e.g., the external test point (TP) shown in Fig. 2, is illustrated as 110. A special bit for providing an EXTERNAL TRIP is stored (written) into the non-volatile memory during manufacture. In performing the EXTERNAL TRIP, the meter status is checked to determine if the KEYBOARD is disabled. If it is not disabled, this subroutine returns error status to the superordinate process and no trip occurs. If the KEYBOARD is disabled, the meter status is again checked to see if it is enabled. If not, error status is returned to the superordinate process. If meter status indicates enabled (MRSTS1.ENAB) is TRUE, we access certain addresses in the non-volatile memory (NVM) to see if the serial number lock (NVM.SERLCK) is TRUE. That is, a specific bit is accessed in the non-volatile memory to determine whether the serial number of the postage meter has been locked in non-volatile memory. If it has not, the trip is executed and normal status is returned to the superordinate process. However, if the serial number has been locked in the non-volatile memory, another address in the non-volatile memory is accessed to determine whether a bit is present to disable the external trip. If so, error status is returned to the superordinate process. However, if a trip lock (NVM.TRPLCK) bit has not been set in non-volatile memory, a trip is executed. Thereafter, control is returned to the superordinate process with normal status.

Referring to Fig. 4, at the end of entry, the Reset Routine illustrated as 120 occurs after the meter has been primed for reset by entry of combination and amount messages. Initially, it is determined whether the meter is in a service state. If so, the service function is executed and control is returned to the superordinate process. If the meter is not in a service state, the meter

status is checked to determine if it is in the privileged state, i.e., the privilege switch for manual postage resetting is operable. Reset in this case is accomplished with a privileged access switch under either wire/metal seal, paper seal, or keylock (same for all meters). With this method "monies" are entered directly into the descending register when the privileged access switch is in the "on" position, i.e., in the privileged state. If it is in the privileged state, a non-volatile memory address NVM.UNIT is accessed to determine if the unit is a meter that has single or double register. If a single register, it is cleared to zero and control is returned to the superordinate process. If the unit is a double register, a further address in a non-volatile memory is accessed to determine if the double register meter is reset via a manual combination NVM.RESET or a non-combination reset. After the reset, control is returned to the superordinate process. If NVM.RESET is set, a manual combination reset is executed and if NVM.RESET is not set a non-combination manual reset is executed. Control is then returned to the superordinate process. Upon reading the state of the meter, if it is determined that it is not in a privilege state, an address in the non-volatile memory is accessed to determine if the value in NVM.UNIT is set to indicate the unit is a double register meter. If it is not set, a procedural error is declared and control is returned to the superordinate process. If it is set to indicate a double register meter, the values are equal and a variable remote meter resetting (VRMRS) is executed and control is returned to the superordinate process.

Thus, it is apparent that the branching resulting from the EXTERNAL TRIP and RESET routines is dependent upon the presence or absence of certain bits in non-volatile memory.

More details regarding the privilege switch, VRMRS and manual reset (combinational or non-combinational) and the routines therefore can be obtained from United States Letters Patent 4,301,507, issued on November 17, 1981, and assigned to Pitney Bowes, Inc. of Stamford, Connecticut.

The functions illustrated in Figures 3 and 4 are illustrative of the present invention. It should be understood that the present invention may be utilized to control firmware branch points in an electronic postage meter to accomplish other functions such as, pre-setting of the registers and ascending register lockout. Preferably, as disclosed in the copending European Patent Application No. 83 102 266.0 (corresponding to U.S. Application Serial No. 355,437, filed on March 8, 1982, in the names of Edward C. Duwel and John H. Soderberg, entitled "Non-Volatile Memory Serial Number Lock for Electronic Postage Meter") and European Patent Application No. 83 106 828.3 (corresponding to U.S. Application Serial No. 397,398 filed on July 12, 1982, in the names of Raymond R. Crowley and John H. Soderberg, entitled "Electronic Postage Meter Having a One Time Actuable Operating Program to Enable Setting of Critical Accounting Registers to Predetermined Values) after the serial number is set in the meter a "one time" program locks up the meter to preclude further changes therein. The disclosures of both these European patent applications are hereby incorporated herein by this reference.

It should be understood for the purpose of the present application that the term postage meter refers to the general class of device for the imprinting of a defined unit value for governmental or private carrier delivery of parcels, envelopes or other like application for unit value printing. Thus, although the term postage meter is utilized, it is both known and employed in the trade as a general term for devices utilized in conjunction with services other than those exclusively employed by governmental postage and tax services. For example, private, parcel and freight services purchase and employ such meters as a means to provide unit value printing and accounting for individual parcels.

It will be apparent to those skilled in the art that various modifications may be made in the present invention without departing from the scope thereof as described in the specification and defined in the appended claims.

Claims:

1. A method of controlling firmware branch points in an electronic postage meter, characterised by the steps of:

storing a program for operation of the electronic postage meter;

providing at least one data bit external to the stored program, the or each such data bit corresponding to a particular branch point in the program; and

selecting a branch of the program for use in operation of the meter in accordance with at least one said data bit so that the program may be readily reconfigured based on the presence of a said data bit.

2. A method according to claim 1 characterised by a plurality of said data bits.

3. A method according to claim 1 or 2 characterised in that the program is stored in at least one ROM (14).

4. A method according to any one of the preceding claims characterised in that at least one data bit is provided to allow reconfiguration of the program to provide for remote tripping of the postage meter.

5. A method according to any one of the preceding claims characterised in that at least one data bit is provided to allow reconfiguration of the program to provide for resetting of the postage meter.

6. A method according to any one of the preceding claims characterised in that at least one data bit is provided to allow reconfiguration of the program to provide for pre-setting of the postage meter.

7. A method according to any one of the preceding claims characterised in that at least one data bit is provided to allow reconfiguration of the program to provide for locking out the ascending register.

8. A method for controlling firmware branch points in an electronic postage meter characterised by the steps of:

storing a program for operation of the electronic postage meter in at least one ROM (14);

setting of a plurality of data bits external to the stored program; and

selecting branches of the program for use in operation of the meter in accordance with the data bits so that the program may be readily reconfigured based on the presence of the data bits.

9. Apparatus for controlling firmware branch points in an electronic postage meter characterised by:

ROM means (14) for storing a program for the electronic postage meter;

non-volatile memory means (24) having addresses therein for storage of information;

at least one data bit for reconfiguring the program stored in a specified address of said non-volatile memory means (24), the or each data bit corresponding to a particular branch of the program; and

means (10,12) interconnecting said ROM means (14) and said non-volatile memory means (24) for providing communication therebetween to reconfigure the program in accordance with the branch of the program selected by at least one said data bit present in said non-volatile memory means (24).

10. Apparatus according to claim 9 characterised in that said interconnecting means includes a system bus (12) and a microprocessor (10).

11. Apparatus according to claim 9 or 10 characterised by a plurality of data bits to reconfigure the program.

12. Apparatus according to any one of claims 9 to 11 characterised in that the presence of at least one said data bit in said non-volatile memory means provides for remote tripping of the postage meter.

13. Apparatus according to any one of claims 9 to 12 characterised in that the presence of at least one said data bit in said non-volatile memory means provides for resetting of the postage meter.

14. Apparatus according to any one of claims 9 to 13 characterised in that the presence of at least one said data bit in said non-volatile memory means provides for pre-setting of the postage meter.

15. Apparatus according to any one of claims 9 to 14 characterised in that the presence of at least one said data bit in said non-volatile memory means provides for locking out the ascending register.

16. Apparatus for controlling the firmware branch points in an electronic postage meter characterised by:

ROM means (14) for storing a program for the electronic postage meter;

a non-volatile memory means (24) having addresses therein for storage of information;

a plurality of flags for reconfiguring the program stored in specified addresses of said non-volatile memory, each of said flags corresponding to a particular active branch of the program; and

interconnecting means including a microprocessor (10) and a system bus (12) for interconnecting said ROM means (14) and said non-volatile memory means (24) for providing communication therebetween to reconfigure the program in accordance with the active branches of the program selected by said flags present in said non-volatile memory (24).

17. An electronic postage meter characterised by apparatus according to any one of claims 9 to 16.

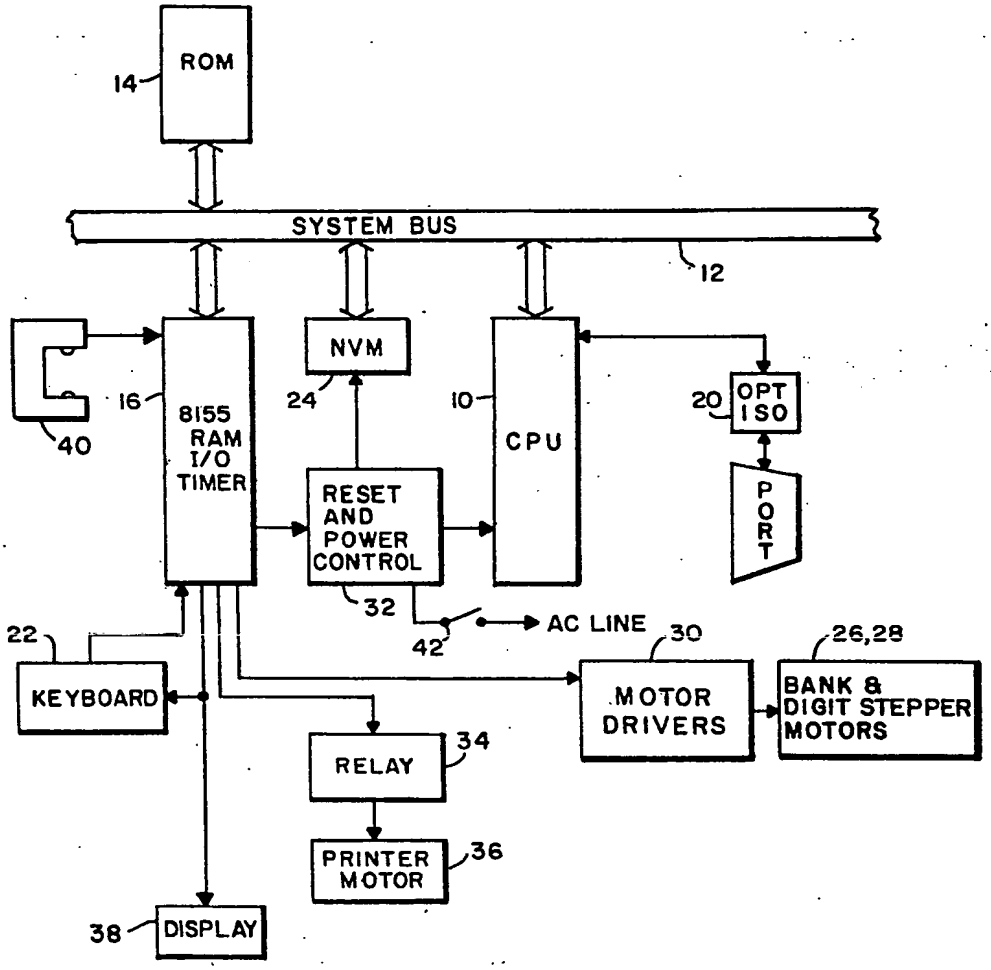

ROM
14
SYSTEM BUS
12
NVM
24
16
8155
RAM
I/O
TIMER
40
10
CPU
20
OPT
ISO
PORT
RESET
AND
POWER
CONTROL
32
42
AC LINE
30
26,28
22
KEYBOARD
MOTOR
DRIVERS
BANK &
DIGIT STEPPER
MOTORS
RELAY
34
PRINTER
MOTOR
36
38
DISPLAY

FIG. 1

Fig. 2a

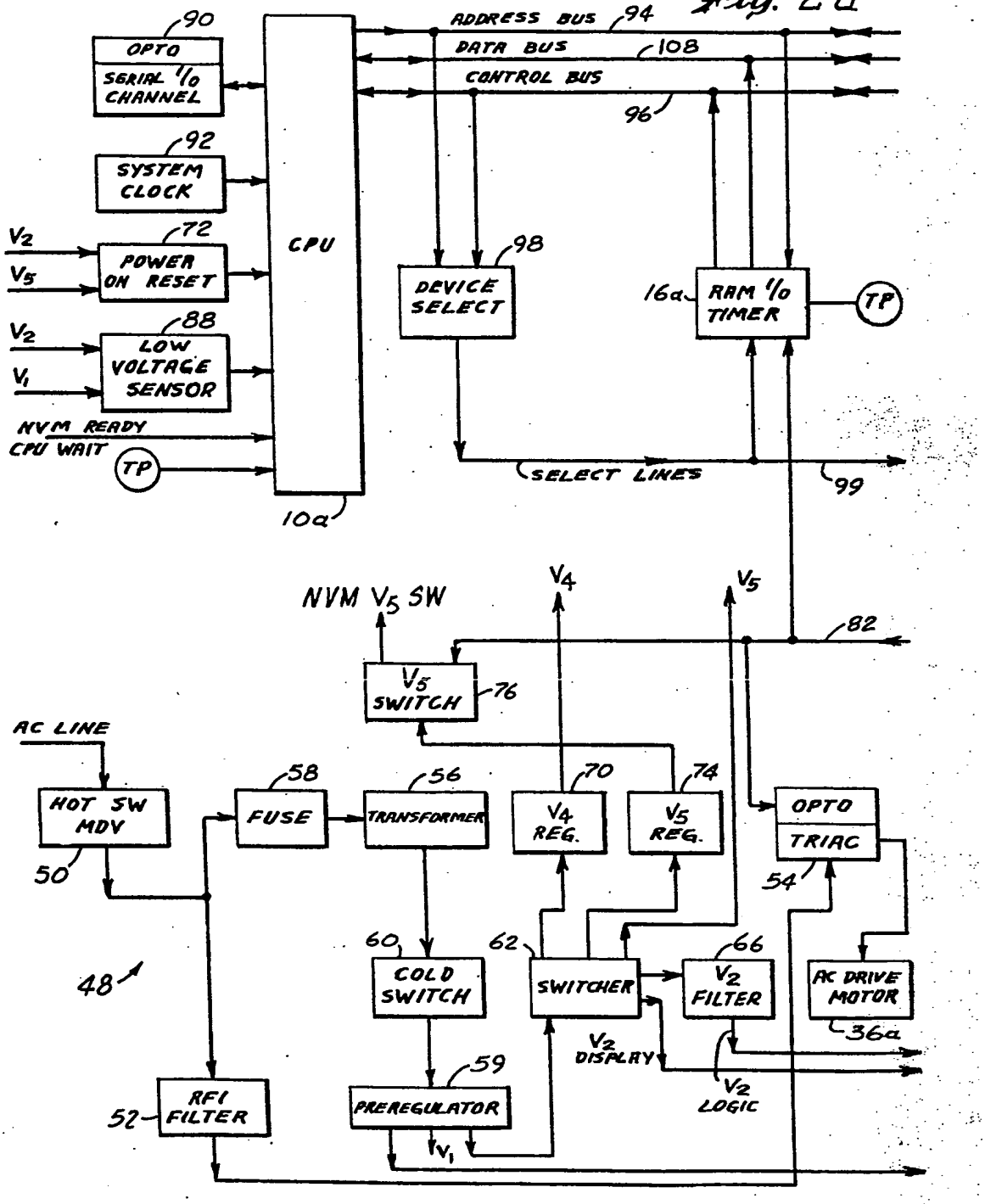
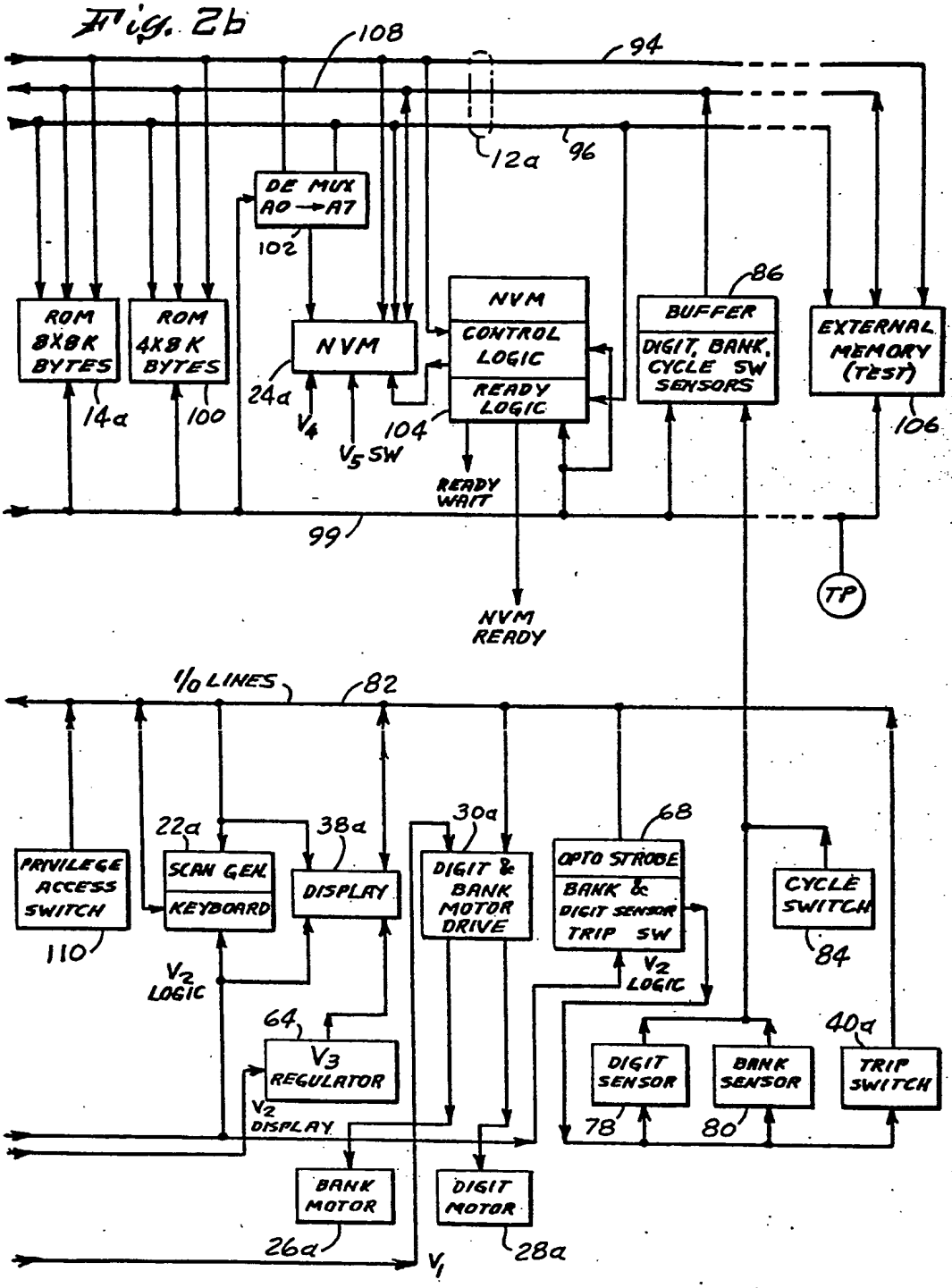

90
OPTO
SERIAL I/O CHANNEL
92
SYSTEM CLOCK
72
POWER ON RESET
88
LOW VOLTAGE SENSOR
NVM READY
CPU WAIT
TP
CPU
10a
ADDRESS BUS
94
DATA BUS
108
CONTROL BUS
96
98
DEVICE SELECT
16a
RAM I/O TIMER
TP
SELECT LINES
99
NVM V5 SW
V4
V5
82
V5 SWITCH
76
AC LINE
HOT SW MOV
50
58
FUSE
56
TRANSFORMER
70
V4 REG.
74
V5 REG.
OPTO TRIAC
54
48
60
COLD SWITCH
62
SWITCHER
66
V2 FILTER
AC DRIVE MOTOR
36a
V2 DISPLAY
V2 LOGIC
59
PREREGULATOR
V1
52
RFI FILTER

Fig. 2b


108
94
96
12a
DE MUX A0 → A7
102
ROM 8X8K BYTES
14a
ROM 4X8K BYTES
100
NVM
24a
V4
V5 SW
104
NVM CONTROL LOGIC
READY LOGIC
READY WAIT
86
BUFFER
DIGIT, BANK, CYCLE SW SENSORS
EXTERNAL MEMORY (TEST)
106
99
TP
NVM READY
I/O LINES
82
22a
38a
30a
68
PRIVILEGE ACCESS SWITCH
110
SCAN GEN.
KEYBOARD
DISPLAY
DIGIT & BANK MOTOR DRIVE
OPTO STROBE
BANK & DIGIT SENSOR TRIP SW
CYCLE SWITCH
84
V2 LOGIC
64
V3 REGULATOR
V2 DISPLAY
40a
DIGIT SENSOR
78
BANK SENSOR
80
TRIP SWITCH
BANK MOTOR
26a
DIGIT MOTOR
28a
V1

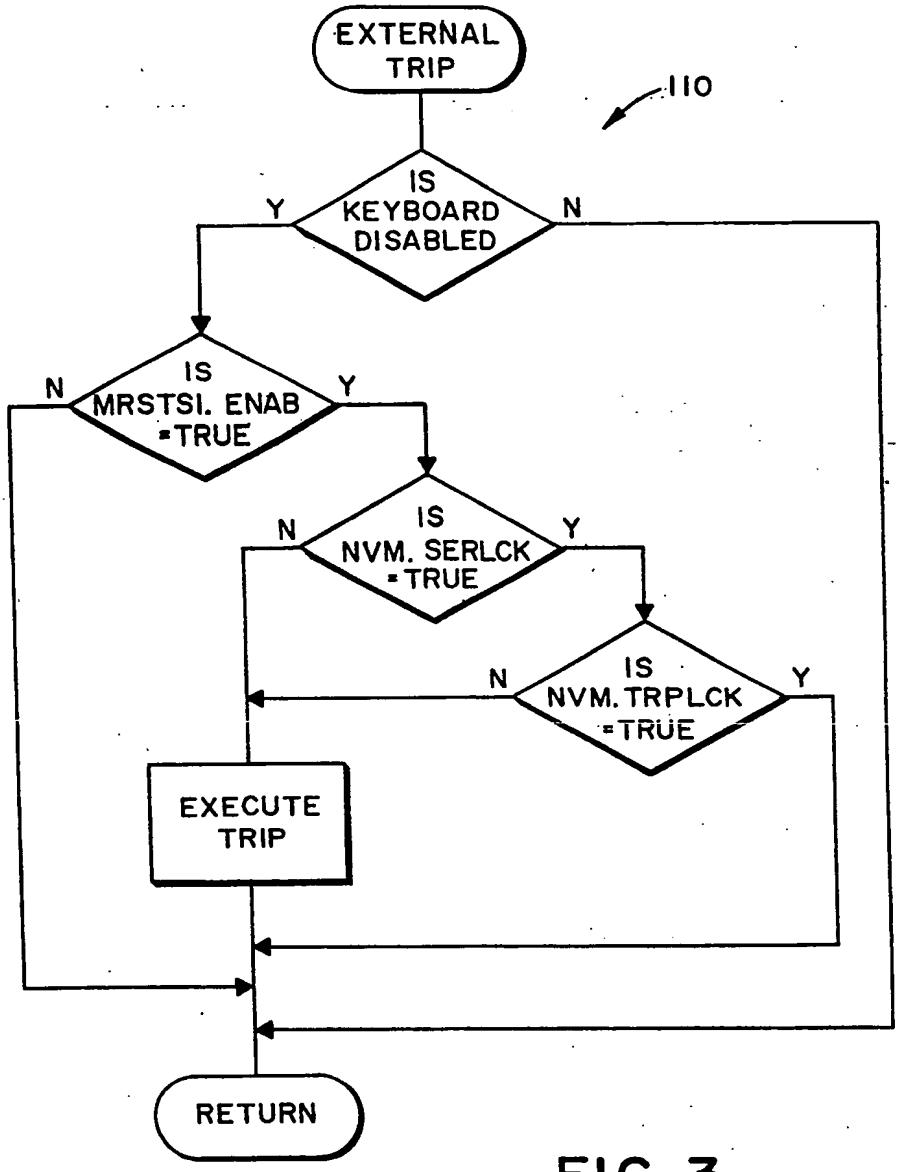

EXTERNAL TRIP
110
IS KEYBOARD DISABLED
Y
N
IS MRSTSI. ENAB =TRUE
N
Y
IS NVM. SERLCK =TRUE
N
Y
IS NVM. TRPLCK =TRUE
N
Y
EXECUTE TRIP
RETURN

FIG. 3

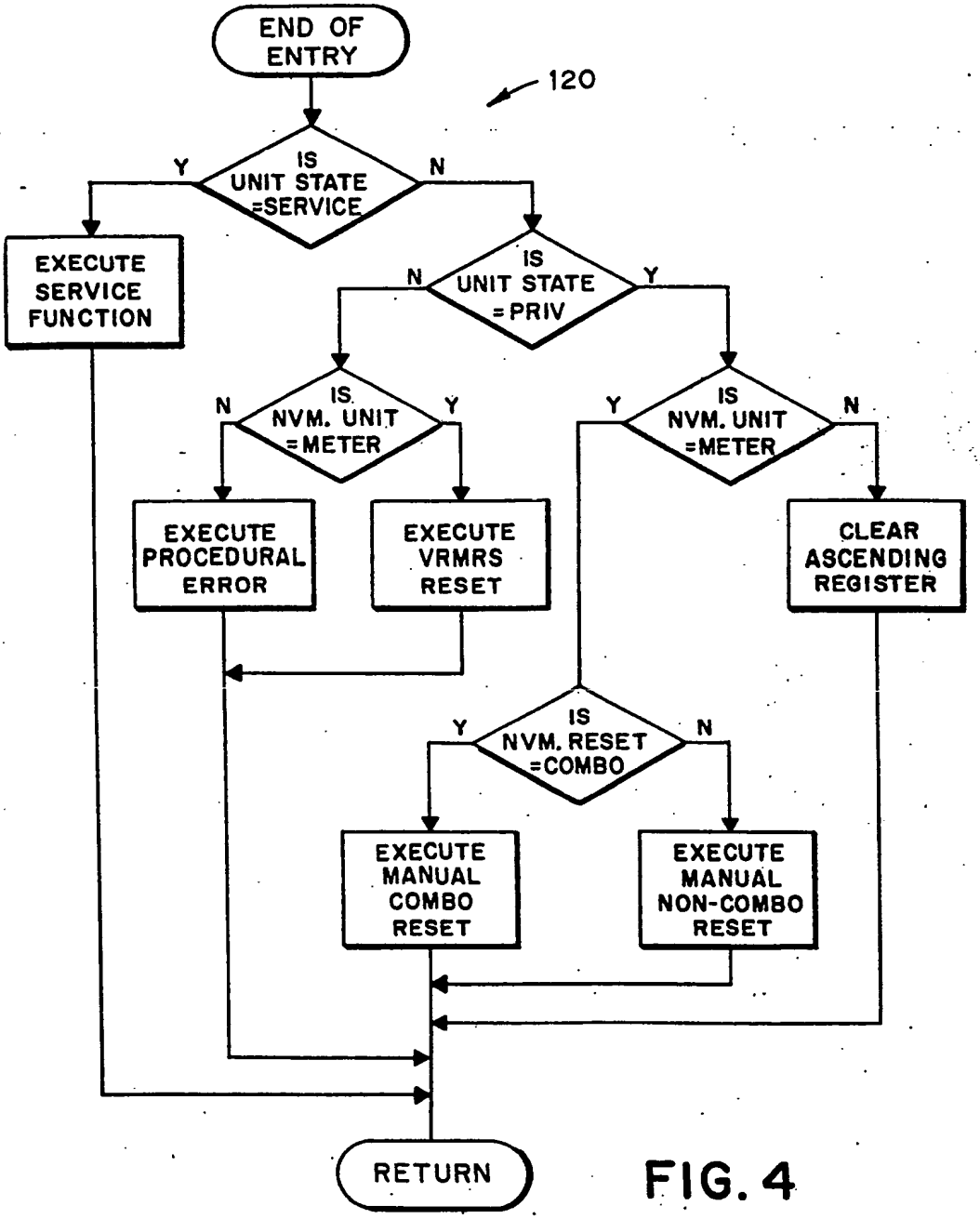

END OF ENTRY
120
IS UNIT STATE =SERVICE
Y
N
EXECUTE SERVICE FUNCTION
IS UNIT STATE =PRIV
N
Y
IS NVM. UNIT =METER
N
Y
IS NVM. UNIT =METER
Y
N
EXECUTE PROCEDURAL ERROR
EXECUTE VRMRS RESET
CLEAR ASCENDING REGISTER
IS NVM. RESET =COMBO
Y
N
EXECUTE MANUAL COMBO RESET
EXECUTE MANUAL NON-COMBO RESET
RETURN

FIG. 4

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